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Notice of Allowability	Application No.	Applicant(s)
	10/658,741	SCHAEFER ET AL.
	Examiner	Art Unit
	Vu A. Le	2824
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to		
2. The allowed claim(s) is/are <u>1-20</u> .		
3. The drawings filed on 10 September 2003 are accepted by the Examiner.		
 4. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b)		
 Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/06 Paper No./Mail Date 02/03/04 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 	6. ☐ Interview Summary (Paper No./Mail Date 8), 7. ☐ Examiner's Amendm	e
		Primary Examiner

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REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance: the present invention relates to a clock circuit used in DDR-DRAM device. The independent claim 1 recites a clock circuit having at least 2 connection, one connection for receiving a differential input clock pulses and/or receiving a single input clock pulse and another connection for receiving the single input clock pulse, wherein the clock circuit further comprises a first and a second pulse relay device, whereby the first pulse relay device is arranged for relaying differential input clock pulses, and the second pulse relay device for relaying a single input clock pulse. The PRIOR ART fails to disclose or suggest such clock circuit as one used in DDR-DRAM device as described in the independent claim 1, therefore, claim 1-20 are in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu A. Le whose telephone number is (571) 272-1871. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vu A. Le

Primary Examiner
Art Unit 2824

03/02/05